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A Low PowerSequential ElementWithHigh Performance ForSynchronous System Design

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***Abstract*—A very low-power high performance power reduction technique, for sequential element has been proposed. As compared with usual FFs, the proposed design technique for the FF reduces power dissipation, when data activity is in low state for long time intervals. This power reduction is found to be the highest among FFs that have been reported in the recent designs. The reduction is achieved by applying dynamic power reduction techniques for an unconventional latch structure. The very small number of transistors, connected to clock signal reduces the power dissipation, and the total transistor count assures a moderate cell area as conventional FFs. Also the fully static full-swing operation makes the cell tolerant of supply voltage and input slew variation. An experimental chip design with 180 nm CMOS technology shows that almost all conventional FFs are replaceable with proposed FF design while preserving the same system performance and a moderate layout area.**

***Index Terms*—Dynamic power reduction,Flip-flops, low-power dissipation, VLSI.**

1) Introduction

The technology market keeps on expanding. In addition to the conventional smart phones, DSLRs, and tablets, development of a variety of wearable information gadgets or healthcare equipment has flourished in recent years. In those kinds of battery-dependent equipment, reduction of power dissipation is a predominant issue, and need for power reduction in VLSI is on the rise daily. Based on such past experiences, lots of circuit technique have been proposed. In VLSI, generally more than half of the power is dissipated in random logic and clock distribution networks. Regarding random logic half of the power is dissipated by elements such as flip-flops (FFs) and latches.

The FFs and latches consume 30-60% of total power dissipated by the system. But in actual chip design, it is not preferable to replace conventional FFs as they guarantee balanced power, performance and cell area. The objective of this paper is to achieve goals such as power reduction without any degradation of timing performance and cell area. In Section 2, we review existing low-power FF. In Section 3, we show our design approach. In Section 4, we propose FF realization with a new methodology.

2) Background

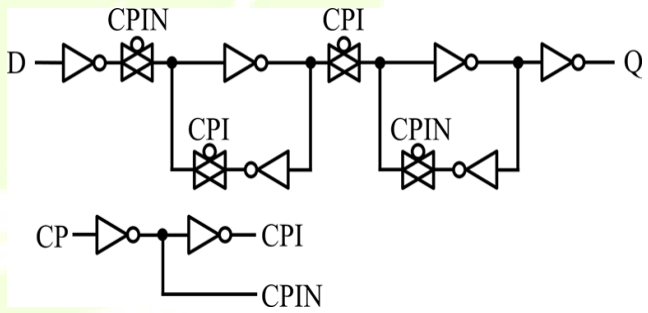

Figure.1 Conventional transmission-gate flip-flop (TGFF) [1].

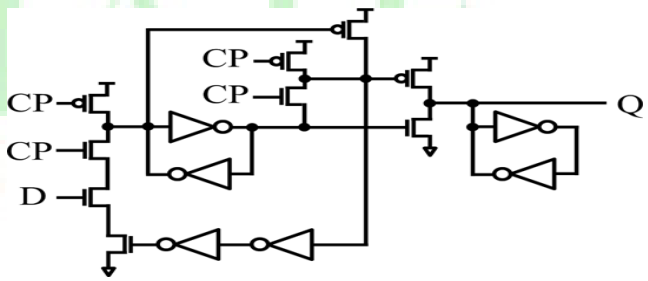

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Figure.2 Cross-charge control flip-flop (XCFF) [1].

The feature of the circuit shown in Fig.2 is that the output transistors are driven separately to minimize charging and discharging of gate capacitance.But during actual operation, some of the internal nodes are pre-set by clock signal when data is high, this dissipates extra power to charge and discharge those nodes, which reduces the effect of power reduction. Driving the output transistors separately will increase the clock load. In the same way circuits including pre-set operation suffer the same problem [1].

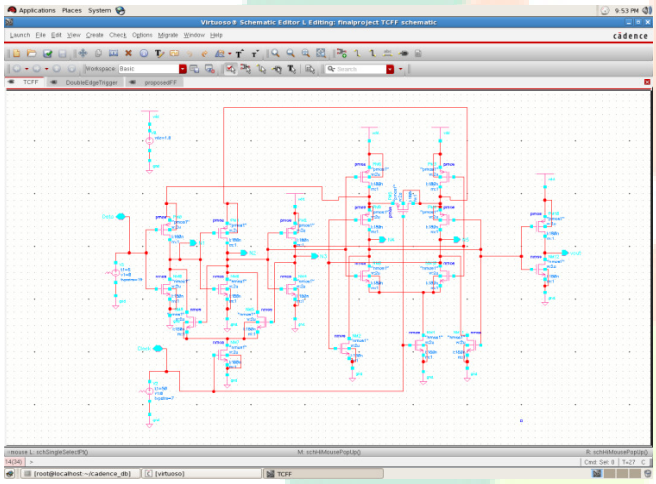

Figure.3 Schematic of Existing TCFF in Virtuoso platform [1]

The transistor level schematic of topologically compressed flip-flop(TCFF) is shown in Fig.3 using the Virtuoso platform for the simulation purpose. It consists of distinct latches in each part. The slave latch(S1,S2) is a commonly used SR(set-reset) latch. But the master latch(M1,M2) is an asymmetrical single data input type. The feature of this circuit is that it operates in a single phase clock. But the clock related transistors count in each latching section is comparatively higher than the conventional flip-flop.

In this part, a review of the hurdles related to existing low power FFs such as conventional TGFF will be discussed. The conventional TGFF is shown in Fig.1.

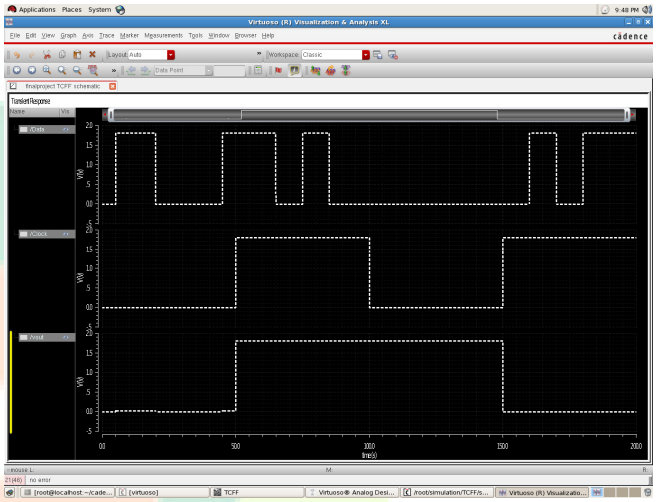

Figure.4 Output timing waveforms of existing TCFF

The timing diagrams of the TCFF are shown in Figure.4. The timing waveforms shows the activity of the FF for the high and low state of data, during rising edge of the clock.

The power waveform for the TCFF is shown in figure.5 and the average power is found to be 131.5µWatt.

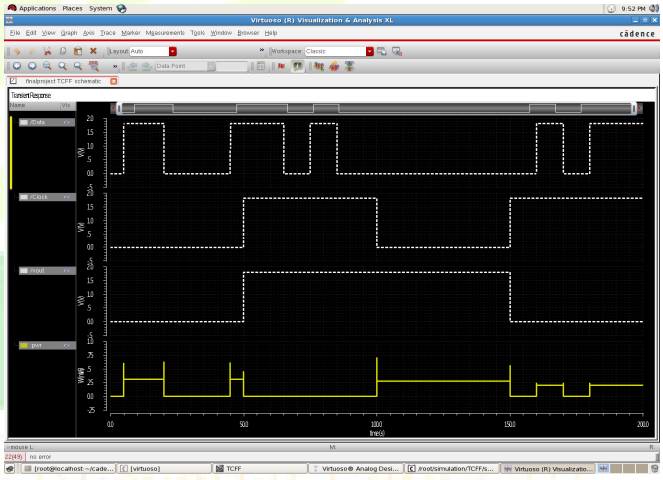

Figure.5 Power waveform for existing TCFF

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This FF is used along with TGFF, when used in a 200-300MHz system, about 98% of TGFF is replaced by TCFF but for a system operating at 333MHz this replacement rate goes down to 88% because of the setup time issue. This setup time issue being a major timing constraint as TCFFs require higher setup time about 105ps as compared to TGFFs with 38ps. Lastly to a system operating at 360MHz the TCFF replacement is not effective and to operate the circuit in such cases transistor resizing is needed.

3) Design approach

To reduce the power dissipation of the FF while maintaining competitive performance, we have tried to implement power reduction techniques which may increase the cell area but not to a greater extent. After analysis of the power and its parameters, we observed that the power dissipation of a FF is mainly because of the transistors operated by the clock signals. But to reduce them directly from the circuit is tedious process. Also keeping in mind that most FFs are operated in only one edge of the clock pulse, operating the FF in both edges of the clock pulse is also a case taken into consideration. Such a technique can be implemented by using both implicit and explicit pulse generator schemes. We have implemented a explicit pulse generator scheme using 180nm technology in Virtuoso platform.

4) Proposed design

After investigating various power principles and the process of power dissipation some of the dynamic power reduction techniques have been found. Some of them are,

- Current comparison based domino logic.
- Precomputation technique.
- Clock controlled self-stabilized voltage control.
- Dual edge triggered pulse generator.

4.1)Current comparison based domino logic

This method is based on comparison of mirrored current of the pull-up network with its worst case leakage current. The proposed circuit technique decreases the parasitic capacitance on the dynamic node, yielding a smaller keeper for wide fan-in gates to implement fast and robust circuits. Thus, the contention current and consequently power consumption and delay are reduced. The leakage current is also decreased by exploiting the footer transistor in diode configuration, which results in increased noise immunity[3].

4.2)Pre computation technique

This technique studies the effectiveness of employingprecomputation in reducing dynamic power consumption incommercial off-the-shelf (COTS) FPGAs. Precomputation is a
high-level logic optimization technique that lowers power consumptionof a design by disabling part of the circuit basedon a few relatively simple precomputation conditions. Withcareful design considerations, the increased logic utilizationand its associated power consumption can be justified by thepower saving resulted from disabling a much larger part ofthe design. Using the designof a comparator as an example, we study the trade-offs andunique opportunities provided by modern FPGA architecturesin employing precomputation as a technique to reduce dynamicpower consumption [5].

4.3)Clock controlled self-stabilized voltage control

CKVdd technique expands the switching power (Psw) functionality for CMOS digital circuits, the Psw is fully turned on only for half of every clock cycle, which means that outer power is fully s upplied to the circuit for half of every clock cycle. Therefore, the CKVdd-circuit is alternatively charged and discharged. When the Psw is turned on to work in the saturation region and then turned offto work in the active resistor region, the progressively rising Vdd iscyclically generated in the synchronous CMOS circuits [4].

4.4)Dual edge triggered pulse generator

The dual edge triggered pulse generator scheme can be characterized into three groups: implicit pulsed dual edge trigger, explicit pulsed dual edge trigger, conventional dual edge trigger. Explicit schemes necessitate a pulse generator section that will be connected to the clock related transistor

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sections of the FF. Implicit schemes use two logic branches receiving a clock and a delayed clock [2]. Figure.6 shows the schematic of dual edge triggered pulse generator.

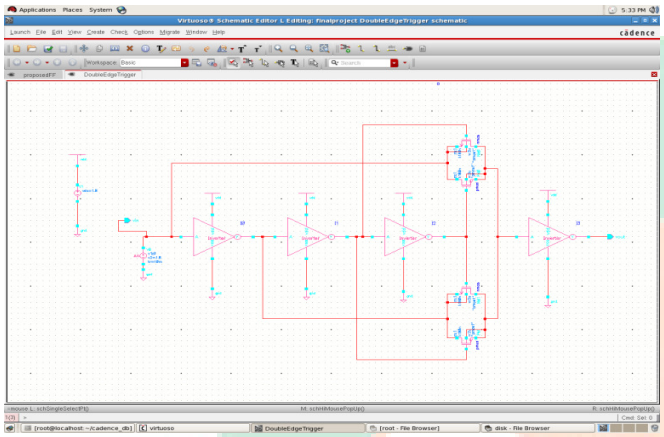

Figure.6 Schematic of Dual Edge Triggered (DET) pulse generator [2].

Of all the methods discussed above, we found the explicit dual edge trigger method to be most convincing for the design to achieve power reduction, as it uses a pulse generator scheme outside the latching part, which could be efficiently used to reduce the power dissipation. The pulsegenerator section produces a short pulse after each clock edge, both rising and falling . During each pulse, latching section becomes transparent and captures theinput data. At all other times, the latch is opaque and the change of the output will not happen. The schematic of the proposed Dual Edge TiggeredTCFF(DET-TCFF) is shown in Figure.7.

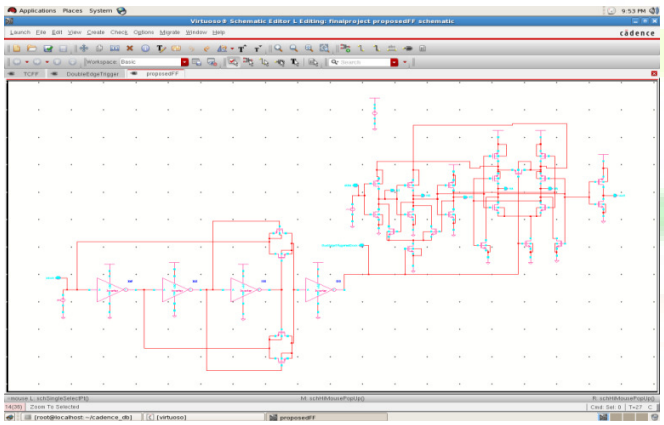

Figure.7 Schematic of proposed DET-TCFF

Design	Average Power in μ Watt
TCFF	131.3
DET-TCFF	112.4

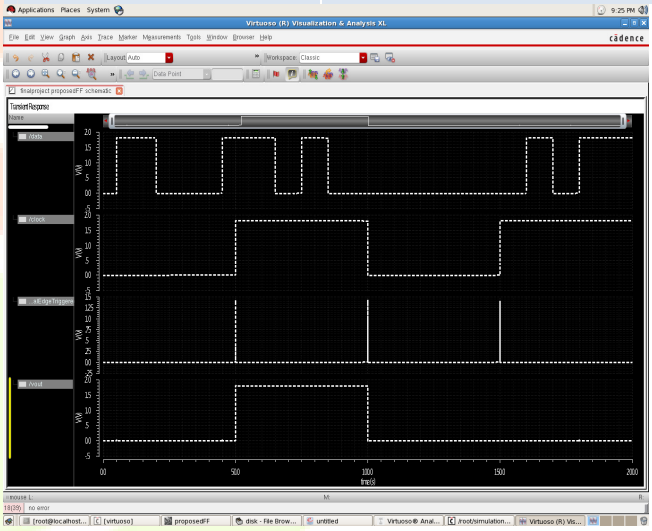

Figure.8 Output timing waveforms of proposed DET-TCFF

In the DET-TCFF, for every edge of the clock pulse, there will be short pulses of equal duration produced by the pulse generator circuit. This in turn will be sent to the clock distribution networks of the FF section. Because of this, the FF will detect the data and make necessary transitions in output from high - to – low, or low - to - high for each pulse as indicated in Figure.8.

From the waveforms it is easily observed that the transition takes place at the rising edge as well as, falling edge of the same clock cycle. This saves a pulse which will minimize the power consumption and reduce delay, thereby increasing the performance of the circuit. The power waveform for the same is shown in Figure.9.

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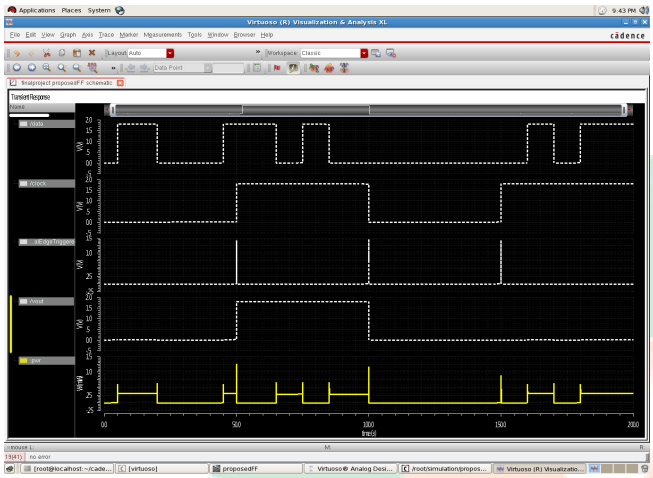

Figure.9 Power waveform for proposed DET-TCFF

The average power consumption is found to be 112.5µWatts. Thus the power consumption has been reduced up to 15% in the proposed design technique than the existing one.

Table.1 Average power in µ Watt.

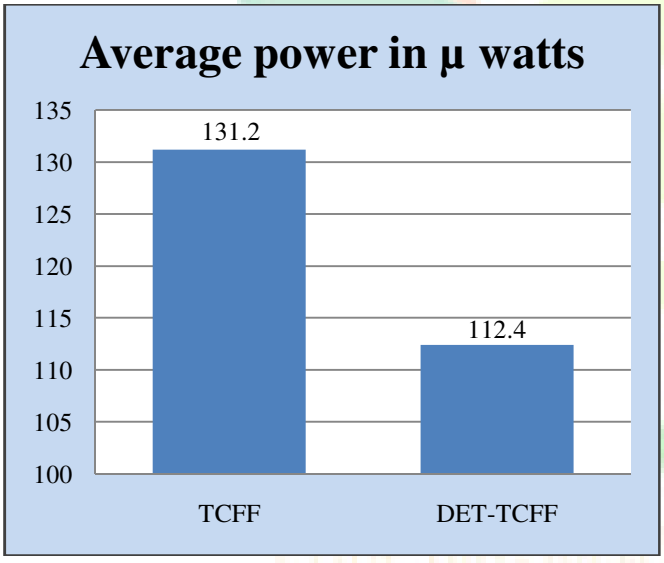

Figure.10 Comparison of Average power.

The power dissipation of the proposed design is very low, typically 15% less compared to the conventional FF design. Thus the topology of proposed method for power reduction can be easily applied to various FFs without any overhead or penalty in performance. This in turn makes the proposed design an easily available replacement for various conventional FF designs.This is evaluated using a 180nm technology using Virtuoso platform and the results have been furnished in table.1 and figure.10. This implies that the design is compatible to be applied for various synchronous sequential system design such as error detectors, phase detectors, peak detectors, frequency dividers, counters, shift registers.

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