ISSN (ONLINE): 2454-9762
ISSN (PRINT): 2454-9762
Available online at www.ijarmate.com

International Journal of Advanced Research in Management, Architecture, Technology and Engineering (IJARMATE)
Vol. 2, Issue 3, March 2016

A Novel 10 Bit Current Steering CMOS Segmented Digital to Analog Converter

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***Abstract*— The design of 10 bit current steering digital to analog converter consisting of a segmented architecture in 90 nm CMOS technology. The resolution for this design is 10 bits, segmented into 6 thermometer encoded current cells and 4 binary weighted current cells. Thermometer encoding is used instead of binary coded decimal to reduce glitches since only one bit changes at a time. The simulation results show the input bandwidth of the DAC is 250 MHz. This work presented a good performance compared with other researches in DNL, INL and Power Consumption also speed. The design methodology of the sub-components such as current cell, thermometer encoder, and bias circuits. A number of different DAC architectures were examined, each with their own advantages and disadvantages. The current steering architecture is the preferred high speed architecture. One of the trades offs in DAC design is the resolution vs. speed. As the resolution increases, it becomes harder to achieve high bandwidth. The resolution for this design is 10 bits.**

***Index Terms*— DAC, current steering, high speed, current cell design.**

I. INTRODUCTION

Data converters are one of the most important types of circuits because they bridge the gap between the analog and digital domains. The speed of the converter is often the bottleneck in high bandwidth applications. As the bandwidth requirements for devices keep increasing, the importance of data converters also rises. High bandwidth digital to analog converters (DAC) have been constructed using processes such as SiGe [1] or GaAs [2] with the prevalence of systems on a chip it is very advantageous to design a high speed converter using standard CMOS processes.

A number of different DAC architectures were examined, each with their own advantages and disadvantages. The current steering architecture is the preferred high speed architecture. One of the trade offs in DAC design is the resolution vs speed. As the resolution increases, it becomes harder to achieve high bandwidth. The resolution for this design is 10 bits. The goal for the DAC is to be able to achieve 400 MHz input frequency, with hopes that higher speeds can be achieved with some circuit optimization. Section II provides an overview of the current steering DAC architecture. More detailed discussion of the sub-components of the DAC is presented in section III. The design of test bench and results of the DAC are described in section IV.

II. 10 BIT CURRENT STEERING DAC OVERVIEW

The current steering DAC works by "steering" the current between a set of differential outputs. Reference currents are created by several current cells and are summed at the outputs [3]. To achieve high speed and to reduce glitches, a binary to thermometer encoder is used [4, 5]. The output from the thermometer encoder turns on the appropriate current cells to produce the analog output. An example of 3 binary bits to 7 bit thermometer code is shown in Table 1. This architecture is Also known as a unary weighted DAC. For high resolution designs the amount of current cells becomes an issue because it increases complexity of the layout [6]. A solution to this problem is to trade off some speed of the fully thermometer encoded design for reduced complexity by segmenting the DAC. This is done by using thermometer encoding for the MSBs and using a binary weighted sub-DAC for the LSBs. For the DAC presented, segmentation was used to obtain 6 thermometer encoded MSBs, and 4 binary weighted LSBs.

TABLE I. BINARY VS. THERMOMETER CODE

Decimal	Binary	Thermometer
0	000	0000000
1	001	0000001
2	010	0000011
3	011	0000111
4	100	0001111
5	101	0011111
6	110	0111111
7	111	1111111

The unit current cells are arranged in a matrix pattern as given in Fig. 1. To control the current cells, two thermometer encoders are used. One encoder addresses the column and the other addresses the appropriate row in the current cell matrix. Since the segmentation for the MSBs is 6, the first three most significant bits (B9, B8, B7) of the inputs are sent to the row encoder, the next three most significant inputs (B6, B5, B4) are sent to the column encoder. With three digital inputs going to the encoder, 8 thermometer outputs are produced. By using this segmentation scheme the DAC has a 8x8 unit

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current cell matrix.

The four least significant bits (B3-B0) digital inputs are sent to the binary weighted sub-DAC. A dummy encoder is placed between the digital input and the current cells to add some delay so the binary weighted and thermometer encoded cells are synchronized. The binary weighted section contains four current cells producing the currents *I*, 2*I*, 4*I*, 8*I*. The output from the binary weighted sub-DAC is connected to the output from the thermometer encoded cells to produce the analog output. Two load resistors are connected to the positive and negative output terminals to convert the output current to voltage. The supply voltage is connected to one end of the load resistor while the current cells are connected with the other end of the resistor. As the current is drawn through the load resistor to the current cells a voltage is created. The final DAC output is found by subtracting the voltage drop across the load resistor from V_{dd}.

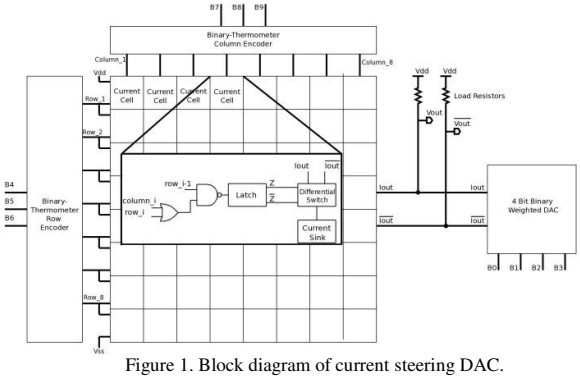

Figure 1. Block diagram of current steering DAC.

The resolution for this converter is 10 bits, which means there will be a maximum of 1024 voltage levels that needs to be produced. The full scale range of the output is from 0 to 725 mV. By dividing 725 mV by 2^{10}, the LSB for the DAC is found to be 0.7 mV. Load resistors are connected to each of the output lines. The resistance is set to be 50 ohm, which creates a unit current *I* of 14 uA. The rest of the current cells produce 28 uA, 56 uA, 112 uA, and 226 uA.

III. Sub-Circuit Design

The current steering architecture has several sub-components that need to be carefully designed. The key component is the current cell, which includes a differential pair of switches, and a current mirror to produce the reference current. The next set of components is the thermometer encoder and local decoders. Finally bias circuits are used to provide the correct bias voltage to all of the current cells.

A. *Current Cell*

The current cells are made up of a pair of differential switches, and a current sink which can be seen in Fig. 2. A single transistor can be used as a current sink, but a cascode current sink is used in this design to increase current sink accuracy. The reference current is created by using NMOS transistors to sink V_{dd} from the load resistors to ground. The switches are controlled by the thermometer encoder and latch circuits. Since the switches are differential only one is turned on at a given time. The input Z turns on transistor M1, allowing current flow from I_{out} to ground. When Z is enabled, Z is turned off directing the current through complementary output Iout. In order to sink the appropriate amount of current a bias voltage is applied to the gate of the current sink. With the cascode current sink two bias voltages are needed.

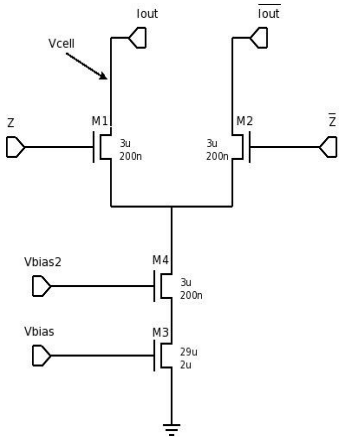

Figure 2. Differential switches and cascode current sinks.

Accuracy of the current mirrors is crucial to the performance of the converter. One issue with the current mirror is that as V_{ds} from M1 to M4 varies, the amount current sinked varies. This is very problematic because the current cells need to output a constant current in order to maintain good accuracy. The output of three different current sink architectures is shown in Fig. 3. The output current is obtained by sweeping the drain voltage seen by the switch (V_{cell}) and current sink transistors in Fig. 3. Since the current cell is directly connected to the output of the DAC, as the output voltage changed, the V_{cell} across the switching transistors and current sinks varies.

The final DAC output is obtained from subtracting the voltage drop across the load resistor by the supply voltage. The voltage divider caused by the load resistors means that the analog output V_{out} will be in the range of 0 to 725 mV. However, the drain voltage across the current cells will operate from 1.2 V to 475 mV. When analyzing the performance of the current cells, 1.2 V in Fig. 3 corresponds to the analog output of 0 V since all of the V_{dd} from the load resistor is being sinked by the current cell. At full scale output, the V_{dd} from the load resistor is split between V_{out} and the current cells, causing the current cell drain voltage to be 475mV.

The first two architectures compared in Fig. 3 are the basic single transistor current sink and the cascode current sink. It was observed that the standard current sink varies 33 uA as V_{cell} changes from 1.2 V to 475 mV. The output current for the cascode current sink changes by 22 uA in the same current cell operating range. The basic current cell does not output a constant current over the operating range. This is caused by

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ISSN (PRINT): 2454-9762
Available online at www.ijarmate.com

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the single transistor current sink having low output impedance. The cascode current sink produces a more constant current since the extra cascode transistor increases the output impedance [7, 8]. The problem with both current sink designs is that as V_{cell} approaches 475 mV, the transistors start to go out of saturation. This causes the reference current to drop which will cause large errors in the DAC output.

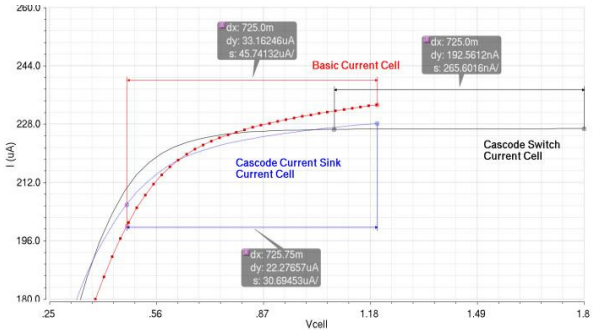

Fig. 3. Comparison of output currents of the different current sink architectures as the drain voltage changes

The current cell design can be further improved by cascoding the switch transistors, which can be seen in Fig. 4. This buffers the switches from the changing output capacitance which reduces glitches and increases switching speed. Charge is stored on the node between the current source and switching transistors [9]. When the switch turns on the capacitance is discharged to the output. The amount of charge dissipated to the output depends on how many current cells are currently active at a given time.

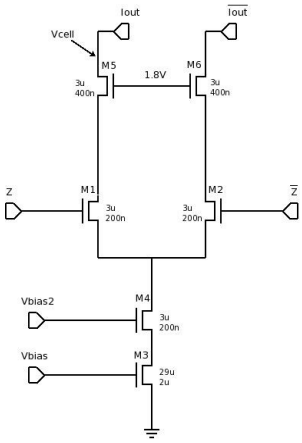

Figure 4. Modified cascode switch current sink.

One of the drawbacks of having a V_{dd} of 1.2 V is that it limits the headroom for the current cells. Even with the cascoded current source there is only a narrow voltage range where the transistors can operate in saturation. A highly accurate current cell is created by modifying the cascade switch transistor seen in Fig 4. To improve the accuracy of the reference current cell, the cascoded switch is replaced with a thick gate oxide transistor [9]. This allows the cascode switch to be biased at voltage higher than the V_{dd} of 1.2 V. A bias voltage of 1.8 V is chosen, increasing the headroom. The higher headroom allows the full-scale DAC output of 725 mV to be achieved by having the current cell operate from 1.075 V to 1.8 V.

The output current of the modified current cell is shown in Fig. 3. This design only varies by 192 nA across the operating range which is a large improvement over the previous two architectures. The accuracy of the DAC reference currents are often measured in how much it deviates from the LSB. The LSB current is typically allowed to be off by plus or minus .5 LSB which is 7 uA in this design. Based on the results in Fig. 4, the basic current sink has an error far greater than .5 LSB. The cascode current sink has an error equal to one LSB. The cascode switch current sink easily meets the requirement of .5 LSB.

In the thermometer encoded section of the DAC, 63 current cells are used, each producing a current of 16*I*. The binary weighted portion contains four current cells, outputting *I*, 2*I*, 4*I*, and 8*I*. The thermometer encoded current cell includes a local encoder circuit, a latch, the current switch, and the current sink. The binary weighted current cell has a latch, current switch, and current sink. To obtain the correct reference current in the different current cells the width of the current sink transistors are adjusted. To increase the current from *I* to 2*I* the current sink transistor width is roughly doubled. Each current cell receives a bias voltage to produce the correct reference current. For the binary weighted and thermometer encoded current cells, the current sink V_{bias} is 450 mV, the current sink cascode transistor Vbias2 is 1.0 V.

B. Current Cell Biased Circuit

Bias circuitry needs to be designed in order to provide the appropriate V_{bias} to the current mirrors. The bias circuit can be localized to each current cell or there can be global bias circuits that supply a large amount of the cells. With the large amount of current cells present having a single bias circuit would mean a large amount of interconnect would be needed. The interconnect could be sensitive to all the switching wires nearby which could cause inaccuracies in the bias voltages. Another consideration for the bias circuit is its sensitivity to power supply fluctuations. A simple voltage reference circuit can be made by using a PMOS as a resistor and a NMOS as a current sink. The downside to this approach is that it is directly dependent on V_{dd}. A more advanced bias circuit is presented in Fig. 5. This design can produce a constant bias voltage even if the power supply varies [7].

The design works by scaling the size of M2 so that is larger than M1. The resistor value is adjusted to obtain the correct reference current. The transistors MSU1, MSU2, MSU3, are added as a start-up circuit. If M1 and M2 are grounded, MSU3 will be enabled, sending current to M1 and M2. Once the bias circuit is in the desired state MSU3 turns off.

ISSN (ONLINE): 2454-9762
ISSN (PRINT): 2454-9762
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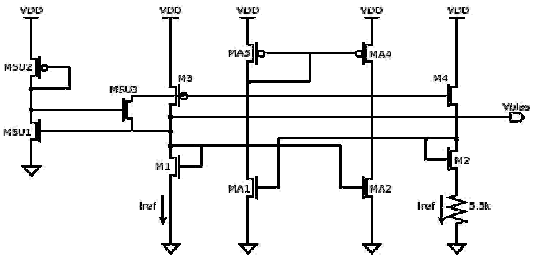

Figure 5. Supply independent bias circuit.

C. *Thermometer Encoding and Local Decoder Design*

Two thermometer encoders are used in the DAC, one to address the columns of the current cell matrix and the other to address the rows. The encoders have three binary inputs and eight thermometer outputs. To obtain the logic for the outputs Karnaugh maps were used. These logic gates were built using standard static CMOS logic.

The encoders can be optimized to reduce delay from the digital input to the current cells. If the static CMOS gates are too slow they could potentially be replaced with pass transistor logic. Buffers are added in some of the gate paths in order to equalize the delay between all the thermometer outputs.

The thermometer encoded current cells all include a local decoder and latch circuits. Fig. 6 shows the logic diagram for the local decoder and latch circuits. The local decoder takes the $column_i$, row_i, and row_{i-1} outputs from the thermometer encoder and determines if the current cell should be turned on. In order to turn on the current cell, row_i or $column_i$ both have to be logic one, which is then sent to an NAND function with row_{i-1}. The decoder logic was implemented in standard static CMOS with an inverter to get the differential signals for the current switches. A high speed master-slave latch was constructed to synchronize all the signals. This is placed between the local decoder and the current switches.

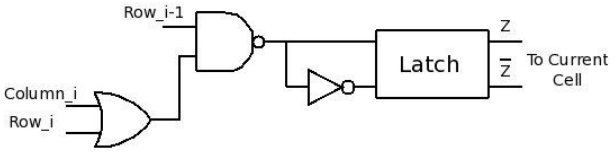

Figure 6. Local decoder and latch.

IV. DAC Results

With all the sub-components completed the DAC was wired together. A 50 ohm load resistor was placed on each of the output lines with one terminal connected to power supply in order to convert the output current into voltage. The plot in Fig. 7 shows the full scale range output of the converter. The clock frequency was set to 500 MHz, and the LSB of the digital input was pulsed at a frequency of 250 MHz.

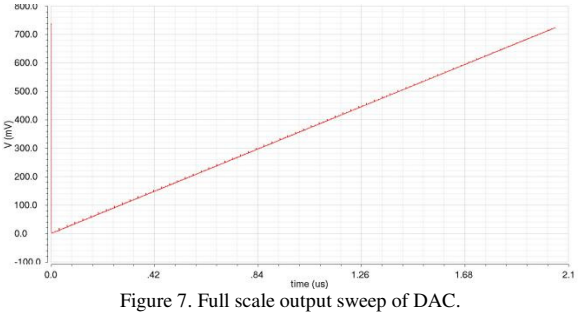

Figure 7. Full scale output sweep of DAC.

The INL and DNL were measured by using modules provided in the ahdlLib library from Cadence. The INL of the converter is seen in Fig. 8 and the DNL is presented in Fig. 9. It can be seen that the max INL is 0.41 LSB and the worst DNL is -0.031 LSB.

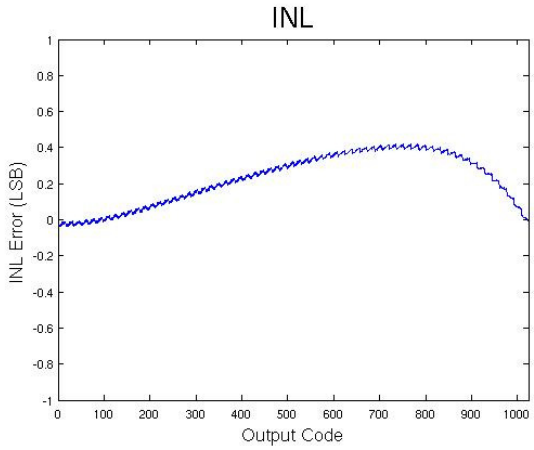

Figure 8. Max INL 0.41 LSB.

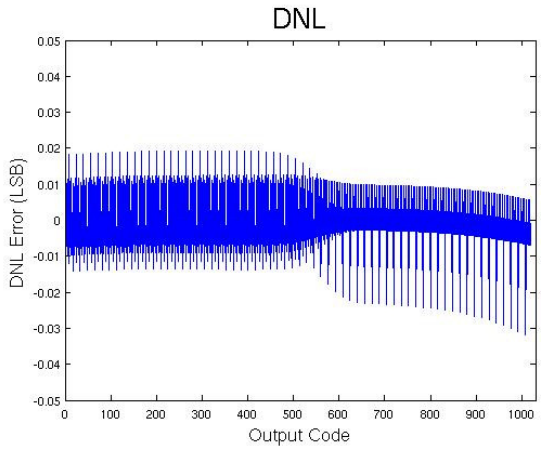

Figure 9. Max DNL -0.031 LSB.

To determine the transient performance of the DAC, the converter needed to reproduce a sine wave. An ideal ADC was created so that a sign input could be given, then the ADC would output the corresponding digital codes to the DAC.

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ISSN (PRINT): 2454-9762
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International Journal of Advanced Research in Management, Architecture, Technology and Engineering (IJARMATE)
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The ideal ADC was created by using a tool built into Cadence called Model writer. This tool allows the user to choose a circuit component, edit the circuits parameters, then it creates the circuit in Verilog-A. A schematic symbol for the circuit component can be made and placed into the DAC design.

Fig. 10 shows the sine input signal and the resulting output from the DAC. The input signals frequency was 125 MHz, while the clock pulsed at 1 GHz. The spectrum plot of the DAC can be seen in Fig. 11. The clock frequency was set to 1 GHz with a sine input of 250 MHz. The SFDR was measured to be 68.62 dB.

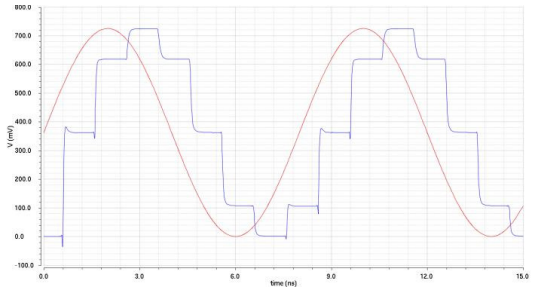

Figure 10. DAC output with 125 MHz sine input.

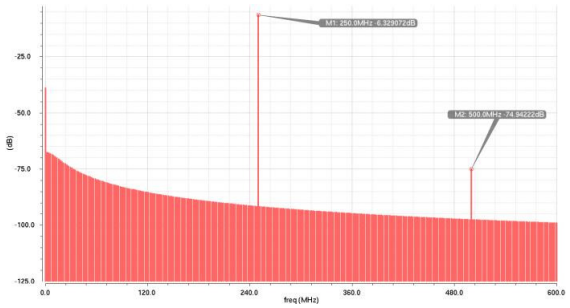

Figure 11. DFT plot of DAC with input frequency of 250 MHz.

V. Conclusion

In this paper the design of a high speed 10 bit digital to analog converter is presented. This design utilizes the current steering architecture in order to operate at high speeds. The design methodology for each of the sub-components was presented. The INL and DNL of the converter were measured to be 0.41 LSB and -0.031 LSB, respectively. The SFDR of the converter was measured to be 68.62 dB with an input frequency of 250 MHz and a clock frequency of 1 GHz.

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References

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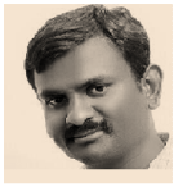

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