IMPLEMENTATION OF AREA EFFICIENT PARALLEL FIR DIGITAL FILTER STRUCTURES USING FAST FIR ALGORITHM

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ABSTARCT

In digital systems, the filters occupy a major role. Implementation of digital filters occupies considerable chip area and consumes significant power during its operation. FIR filter are widely used in circuits for their stability but they have significant dynamic power dissipation. FIR filter have a constant co efficient and multiply it with input signal to generate its output. Multipliers used in FIR architectures consume more power and large area than the adders. This work describes the design of parallel FIR filter structures using minimum number of multipliers and low power adders. This filter structure uses adders instead of multipliers since the adder require low power and less area than the multipliers. Moreover, number of adders does not increase along with the length of parallel FIR filter. The FIR filter was synthesized implemented using Xilinx ISE V10.1 and FPGA to target device.

KEYWORDS:*Digital signal processing (DSP), Fastfinite-impulse response (FIR) algorithms (FFAs), Parallel FIR, Symmetric convolution,*

I.INTRODUCTION

Digital signal processing (DSP) has many advantages over analog signal processing. Digital signals are more robust than analog signals with respect to temperature and process variations. The FIR digital filter is one of most widely used fundamental devices performed in DSP systems. In atypical digital filtering application, software running on a digital signal processor (DSP) reads input samples from an A/D converter, performs the mathematical manipulations dictated by theory for the required filter type, and outputs the result via a D/A converter. Many algorithms are known to reduce the arithmetic Complexity of FIR filtering.

Finite-Impulse Response (FIR) filters have been and continue to be important building blocks in many digital signal processing (DSP) systems. Due to the increase of portable battery-powered wireless systems in recent years, such as cellular phones and pagers, low power and small area digital filter designs have become more and more important.

High-performance and low-power digital signal processing (DSP) is more useful in multimedia application, because it has explosive growth. In any digital signal processing (DSP) system, the FIR filter is one of the fundamental processing elements for giving high performance. FIR filters are used in DSP applications such as video and image processing to wireless communications. In video processing, the FIR filter circuit has the tendency to operate at high frequencies and other applications, like cellular telephony and multiple-input multiple-output (MIMO), the FIR filter circuit can be operate in moderate frequencies and also has low-power circuit with high throughput.

Two techniques of DSP applications like parallel and pipelining processing are used to reduce the power consumption. Power consumption of the original filter is reduced by parallel or block processing with digital FIR filters and also throughput is increased. Multiple outputs of parallel processing are computed by parallel in a clock period. So the level of parallelism increases the effective sampling speed. In the parallel processing applications, hardware units are replicated by involvement of an FIR filter and parallel functions of several inputs with several outputs can be processed at the same time.

The original circuit area is A, and the L-parallel circuit needs an area of L × A. Linearly increases the circuit area with the block size. Due to the design area limitations, parallel processing hardware has much trouble in design situations. So the trouble can be solved by use of parallel FIR filtering structures that consume less area than traditional parallel FIR filtering structures.

Critical path is reduced due to the pipelining transformation that is introducing pipelining latches along the data path and also it increase the clock speed or sample speed or to reduce power consumption at same speed. Power consumption can be reduced by pipelining as similar to the parallel processing.

II.OVERVIEW OF THE FFA ALGORITHM

With the continuing trends to reduce the chip size and integrates multichip solution into a single chip solution it is important to limit the silicon area required to implement parallel FIR digital filter in VLSI implementation. The Need for high performance and low power digital signal Processing is getting increased. Finite Impulse Response (FIR) filters are one of the most widely used fundamental devices performed in DSP system.

General form (traditional algorithm)

Consider an N-tap FIR filter which can be expressed in thegeneral form asN-1

$$Yn=\Sigma\ hi\ xn\text{-}i\ ,\ n=0,1,2,\ldots,\infty \quad (1)$$

Where {x (n)} is an infinite-length input sequence and {h(i)} are the length-N FIR filter coefficients. This block FIRfiltering equation shows that the parallel FIR filter can be realized using *L*2-FIR filters of length *N/L*. This linear complexity can be reduced using various FFA structures.

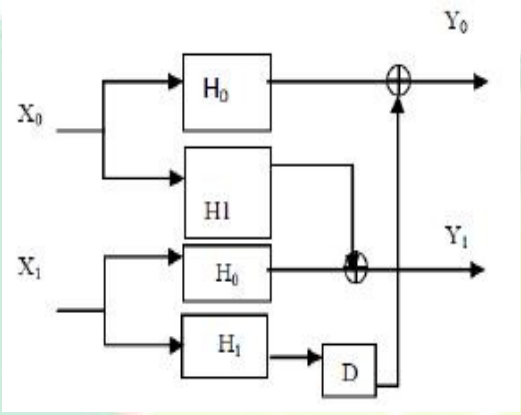

Fig 1: Traditional 2X2 Parallel FIR filterImplementation

2 X 2 FFA-1 approach (L = 2)

The (2X2) FFA results in a filtering structure are shown. At first it may seem that (2X2) uses 5 filtering operations since Y0 requires 2multipliers (filtering operations) and *Y1* requires 3multipliers. However, *X0H0*and *X1H1* are found in both *Y0* and *Y1*. These two terms need only to be computed once which means that the total number of filtering operations is 3. This means that the (2X2) FFA structure uses 3(*N*/2) multipliers and 3(*N*/2–1)+4 adders.

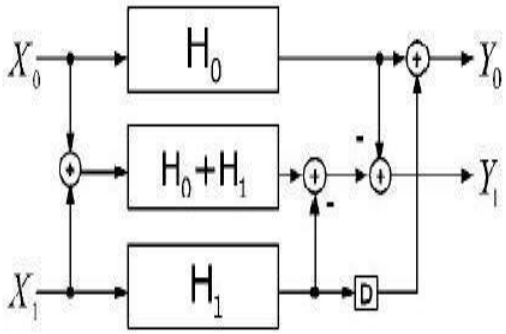

Fig -2: Parallel FIR filter Implementation

III.PROPOSED FFA STRUCTURES FOR SYMMETRIC CONVOLUTIONS

FFA-2 APPROACH

A new structure is proposed to utilize the symmetry of coefficients. Poly-phase decomposition is manipulated to earn many sub-filter blocks, which contain the symmetric coefficients. The sub-filter block reuses the half the number of multiplications and the total amount of an N-tap L-parallel FIR filter with saved multipliers uses the half the number of multiplications in a single sub-filter block (N/2L).

When it comes to a set of even symmetric coefficients, this can earn one more sub filter block containing symmetric co- efficient, the first FFA approach parallel FIR filter.

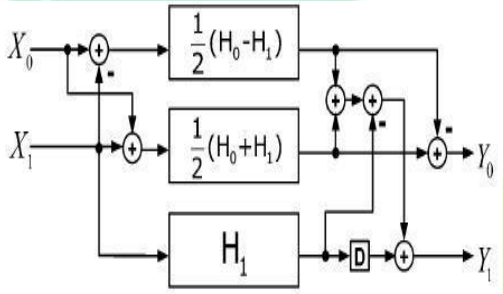

Fig 3: Implementation of the two-parallelFIR filter.

IV.COMPARISON BETWEEN BOTH APPROACH FFA-1 & FFA-2

Comparison of first and the second FFA structures Number of required multipliers (m.)reduced Multipliers (r.m.), number of required adders in Sub filter section (sub.), number of required adders , In pre/post processing blocks (pre/post.), number of The increased adders (i.e)

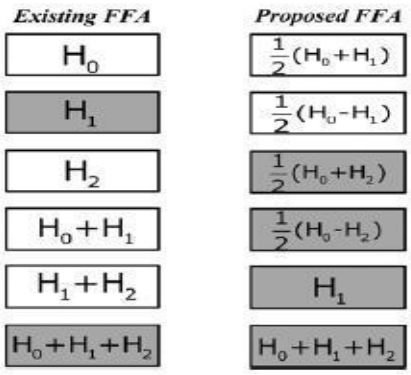

Fig 4: Comparison between sub filter block of bothstructure

As shown from the given example, after applying the second structure , four out of six sub filter blocks,i.e., *H*1, *H*0 + *H*2,H0-H2, *H*0 + *H*1 + *H*2, are with symmetric coefficients now, whichmeans a single sub filter block can be realized in Fig. 6, with only half the amount of Multipliers required. Each output of multipliers responds to two taps, except the middle one. Note that the transposed Direct-form FIR filter is employed. Compared with the first structure FFA three-parallel FIR filter structure, the second structure leads to two more sub filter blocks, which contains symmetric coefficients. Therefore, for an *N*-tap three parallel FIR filter, the second structure can save *N*/3 multipliers from the first FFA structure. However, it comes with the price of the increase in amount of adders, i.e., five additional adders, in preprocessing and post processing blocks.

V.CONCLUSION

In this paper, we have reviewed parallel FIR filter structures, which are beneficial to symmetric convolutions when the number of taps is the multiple of 2 or 3.Multipliers are the major portions in hardware consumption for the parallel FIR filter implementation. The second structure exploits the nature of even symmetric coefficients and save a significant amount of multipliers at the expense of additional adders. Since multipliers outweigh adders in hardware cost, it is profitable to exchange multipliers with adders. Moreover, the number of increased adders stays still when the length of FIR filter becomes large, whereas the number of reduced multipliers increases along with the length of FIR filter. Consequently, the larger the length of FIR filters is, the more the second structures can save from the first FFA structures, with respect to the hardware cost. Overall, in this paper, we have provided new parallel FIR structures consisting of advantageous poly-phase decompositions dealing with symmetric convolutions comparatively better than the first FFA structures in terms of hardware consumption. So, now apply this idea we can implement a new technique which reduces more multipliers and can reduces more system cost.

VI.RESULTS AND OUTPU

The coding has been written in Xilinx ISE V10.1 and it is connected to the FPGA Spartan 3E kit .The connections are shown in the Fig 5.

Fig 5: Connection of FPGA kit with PC

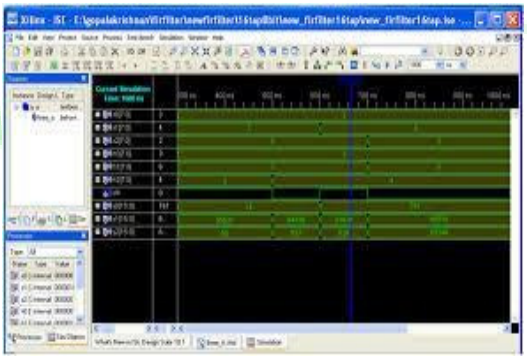

Fig 6: Output waveform of two-parallel 72 tap FIRfilter

The output waveform of the two parallel 72 tap FIR filter is obtained by fetching the input sequences to reduce the power and to obtain the area efficient parallel digital FIR filter.

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